19. (currently amended) A system for erasing one or more non-volatile memory ("NVM") cells comprising: A NVM array, and an erase pulse source to produce an erase pulse having a predominantly non-flat and non-linear voltage profile, and wherein said erase pulse source is adapted to produce an erase pulse having a predefined voltage profile selected from the group consisting of ramp-like, exponential-growth-like, asymptote-like and stepped.

Claim 4, line 1 changes "claim 3" To - -claim 1- - SB 9-4-09

Cancel Claims 2, 3, 10 and 11.

Allowable Subject Matter

4. Claims 1, 4 – 9 and 12 - 19 are allowed.

5. The following is an examiner's statement of reasons for allowance:

With respect to claim 1, the prior art of record fails to anticipate or render obvious a method of erasing one or more non-volatile memory ("NVM") cells, in combination with other limitations, comprising: "wherein said erase pulse has a predefined voltage profile selected from the group consisting of ramp-like, exponential-growth-like, asymptote-like and stepped."

With respect to claim 9, the prior art of record fails to anticipate or render obvious a circuit for erasing one or more non-volatile memory ("NVM") cells, in combination with other limitations, comprising: "wherein said erase pulse source is